Remarks

Claims 1, 2, 6-11, 13-15, 18 and 19 are pending in the application. Claims 1, 2, 6-11, 13-15, 18 and 19 have been rejected under 35 U.S.C. § 102(b). In view of the following remarks, reconsideration and withdrawal of these grounds of rejection is requested.

Claim Objections

Claims 9 and 19 stand objected to because the Examiner contends the term "series transistor" lacks antecedent basis in the claims, and because parentheticals appear in claim 9. Claims 9 and 19 have been amended, and thus reconsideration and withdrawal of this objection is respectfully requested.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 2, 6-11, 13-15, 18 and 19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by one of Inamori et al. (U.S. Pat. No. 6,229,370), Crampton (U.S. Pat. No. 5,767,721) or Cho et al. (U.S. Pat. No. 6,496,072). For the reasons set forth below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

The present invention comprises, in one exemplary embodiment, a switch 40 including a series switching transistor 42 and a shunt transistor 46. A signal path 51 couples a Radiofrequency (RF) input port 12 to an RF output port 14. A first control voltage V_{HI} is coupled to the signal path 51 near the input port 12. A second control voltage V is coupled to the series switching transistor 42 at its gate, and to the shunt transistor 46. The shunt transistor 46 is

coupled to a feedforward capacitor 48 which assists in enhancing the isolation between input port 12 and output port 14, and improving the harmonic noise rejection of the switch 40.

In operation, when the second control voltage V is above the pinchoff voltage (V_p) of the series switching transistor 42 (e.g., V_{p24}), the series switching transistor 42 is turned ON and the shunt transistor is turned OFF. Alternatively, when the second control voltage V is below the pinchoff voltage of the series switching transistor (V_{p24}) and the first control voltage V_{HI} is greater than V_{p24}, the series switching transistor 42 is turned OFF and the shunt transistor is turned ON. For example, if V_{p24} were 2 Volts, any second control voltage V above 2 Volts would bias series switching transistor 42 ON and bias shunt transistor OFF. Similarly, if the second control voltage V dropped to zero (0) Volts, and V_{HI} were maintained above V_{p24} at all times (e.g., at say 5 Volts), the series switching transistor 42 would be biased OFF and shunt transistor 46 would be biased ON. Thus, both the series switching transistor 42 and the shunt transistor 46 may be controlled by a single control signal (e.g., the second control signal V), an action which could not have been accomplished by the prior art circuit shown in Figure 1 (which includes two control voltages V and V').

Independent claim 1 now recites:

> An integrated circuit switch comprising: at least two signal ports coupled by a signal path, the signal path including a channel of at least one series FET; a shunt path coupled to ground and including a channel of a shunt FET; a first control voltage applied to the signal path; and, a second control voltage applied to a gate of the series FET and to a drain/source of the shunt FET, wherein the shunt path includes at least one feedforward capacitor. [emphasis added].

Thus, claim 1 now requires a circuit including a "first control voltage" applied to a signal

path which includes a "series FET," and a "second control voltage" applied to the gate of the series FET and the source or drain of a "shunt FET." Claim 1 also requires at least one "feedforward capacitor" coupled to the shunt FET. None of Inamori, Crampton or Cho discloses, teaches or suggests such an invention.

Inamori teaches an amplifier including a signal line 74 with input 14 and output 15, and variable resistors 71-73 (See Fig. 2). A gain control voltage Vc is applied to the sources of variable resistors 72, 73 and to the gate of variable resistor 71. Inamori does not disclose, teach or suggest a "first control voltage" applied to the signal line 74, or a "feedforward capacitor" coupled to a shunt FET.

Crampton teaches a switch circuit 56 with an RF input 58 and an RF output 70. The switch circuit 56 also includes depletion mode FETs 64, 80 which are coupled to a control voltage V1. Crampton does not disclose, teach or suggest a "first control voltage" applied to the signal line connecting the RF input 58 to the RF output 70. Additionally, Crampton does not disclose, teach or suggest a "feedforward capacitor" coupled to FET 80. In fact, the only capacitors coupled to FET 80 are isolation/coupling capacitors 74, 84 (emphasis added).

Cho teaches an amplifier which couples an antenna 110 to a logic controller through an Low Noise Amplifier (LNA) 108. The amplifier includes FETs 201, 202 which are biased by a control signal V_{cont}. Cho does not disclose, teach or suggest a "first control voltage" applied to the signal line connecting the antenna 110 to the logic controller. Cho also does not disclose, teach or suggest a "feedforward capacitor" coupled to FET 202. Again, the only capacitor coupled to the FET 202 is isolation/coupling capacitor 203 (emphasis added).

Accordingly, because none of the cited references disclose, teach or suggest a switch circuit including a "first control voltage" applied to a signal path which includes a "series FET," and a "second control voltage" applied to the gate of the series FET and the source or drain of a "shunt FET," where the shunt FET is coupled to a "feedforward capacitor," reconsideration and withdrawal of this ground of rejection with respect to independent claim 1, is respectfully requested.

Independent claims 2, 8 and 9 have been amended to include similar limitations to those discussed above with reference to claim 1. Therefore, for at least those reasons discussed above with respect to claim 1, reconsideration and withdrawal of this rejection with respect to claims 2, 8-11, 13-15, 18 and 19 is also respectfully requested.

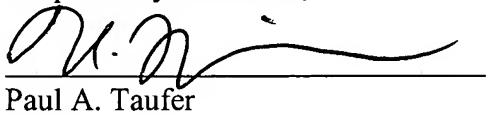
Independent claim 6 included limitations upon filing directed toward "means for enhancing the isolation between the first and second ports, and for improving the harmonic noise rejection of the switch" which are not disclosed, taught or suggested by the cited references (emphasis added). As the Examiner is well aware, 35 U.S.C. § 112, Paragraph Six entitles patent applicants to define claim limitations by 'means plus function' language, and the recited function cannot be disregarded in examination. See, M.P.E.P §§ 2182 ("...the application of a prior art reference to a means or step plus function limitation requires that the prior art element perform the identical function specified in the claim) and 2183 (Establishment of prima facie case requires the prior art element: "(A) performs the function specified in the claim..."). Nowhere do Inamori, Crampton or Cho disclose, teach or suggest means for "enhancing isolation" and "improving harmonic noise rejection."

Additionally, claim 6 has been amended to include a limitation of a "second control signal input" coupled between the first port and the second port. As discussed above with reference to independent claim 1, none of the cited references disclose, teach or suggest a voltage control signal coupled to an RF signal line. Accordingly, reconsideration and withdrawal of this ground of rejection with respect to claims 6 and 7 is respectfully requested.

Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

Respectfully submitted,



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